REMARKS

Claims 21-25 and 31-32 are pending. Applicant's invention is directed to a method of making a semiconductor device and in one embodiment includes forming a conductive layer having a topography that includes a substantially vertical component, forming an overlayer, etching a contact hole in the overlayer in an overetch amount into the substantially vertical component of the conductive layer, and forming a contact in the hole adjacent to and directly contacting the vertical component of the conductive layer.

In the most recent Office Action, the Examiner rejected claims 31-32 under 35 USC §112, ¶2 as indefinite. Specifically, the Examiner objected to the language "forming a contact in said overlayer ..." in claim 31. Applicant has now amended claim 31 to clarify that language. The claim now recites that a contact hole is formed in the overlayer and that the contact hole is then filled with a conductive material. Basis for the amendment is found in the specification at page 8, lines 21-23, and is shown in Figs. 6 and 7. Applicant submits that claims 31-32 as amended are definite and in compliance with §112 of the statute.

Also in the Office Action, the Examiner rejected claims 21-24 and 31-32 under 35 USC §102(e) as anticipated by Zamanian. Zamanian teaches a semiconductor integrated circuit having an improved landing pad. Referring to Fig. 6, Zamanian teaches an oxide layer 28 that includes an opening 30 formed through the oxide layer 28. A polysilicon layer 32 is formed over the oxide layer 28 and the contact opening 30. A silicide layer 36 is formed over the polysilicon layer 32. A barrier layer 34 is formed over the silicide layer 36. A dielectric layer 40, contact opening 42, and conductive contact 44 are formed, wherein barrier layer 34 is located in the bottom of the contact opening underlying the aluminum layer 44. See col. 5 lines 49-63.

Applicant notes that the Examiner is no longer relying upon the Fig. 5 embodiment of Zamanian. Rather, only the Fig. 6 embodiment is relied upon to reject the claims. Claim 21 has been amended to recite that the layer of conductive material is formed in the opening of the underlayer and that the contact hole is etched in the overlayer and in an overetch amount of the substantially vertical component of the layer of conductive material in the opening. Basis for this amended language is found in the

specification with reference to Figs. 6 and 7, beginning at page 8, line 21, and continuing onto page 10.

Zamanian does not teach or suggest such a method. As understood, the Examiner is asserting that barrier layer 34 corresponds to the claimed layer of conductive material, and that Zamanian describes in column 6 that a portion of barrier layer 34 may be etched away during formation of the contact opening. However, if barrier layer 34 is the "layer of conductive material," then it does not have a substantially vertical component "in said opening" as recited in amended claim 21. Accordingly, Zamanian does not teach each and every element of the claimed invention and cannot anticipate claim 21, and claims 22-25 which depend therefrom.

Alternatively, if the Examiner is asserting that polysilicon layer 32 is the "layer of conductive material," then it is not etched at all during formation of the contact hole and cannot meet the claim language. For all of these reasons, applicant submits that Zamanian does not anticipate claims 21-24.

Claim 31 as amended recites that the contact hole is formed in the overlayer and in the vertical component of the layer of conductive material in the opening. Claim 31 also recites that the contact hole is disposed adjacent to and directly contacts the vertical component of the conductive material in the opening. Again, basis for this amended language is found in the specification with reference to Figs. 6 and 7, beginning at page 8, line 21, and continuing onto page 10.

Zamanian's barrier layer 34 in the Fig. 6 embodiment, if asserted to correspond to the claimed "conductive layer," does not fill the opening as recited. If polysilicon layer 32 is considered to be the "conductive material," then no portion of the contact hole is formed in layer 32, and the contact hole does not directly contact that layer. Zamanian does not anticipate claim 31 because Zamanian does not show each and every element of the claimed invention. For all of these reasons, applicant submits that claim 31 as amended, and claim 32, which depends therefrom, are patentable over Zamanian.

Also in the Office Action, the Examiner rejected claims 31-32 under 35 USC §102(e) as anticipated by Okada. The Examiner asserts, *inter alia*, that the structures formed in Okada's Figs. 2A-C and 3 show the steps of forming a structure having an

opening, filling the opening with a layer of conductive material 9, forming a contact hole 11 in an overlayer 10 and "over said layer of conductive material." The Examiner asserts that contact 12 is formed in the opening in overlayer 10 "and in the vertical component disposed adjacent to and contacting the vertical component of the layer of conductive material 9."

The Examiner's interpretation of Okada is faulty. Okada does not teach forming a structure having an opening in a semiconductor layer and filling the opening with a layer of conductive material. The layer of conductive material 9 shown in Okada's Figs. 2A-C and 3 simply lies upon the semiconductor structure. Contact holes 6 and 6a are filled by electrode material 7a and 7b. An insulating film 8 then overlies the electrodes. Conductive layer 9 is deposited over film 8. No "openings" in film 8 are filled with any conductive material 9.

Further, contacts 12 extend only to the surface of conductive layer 9 and do not extend into any vertical component of the conductive layer 9 as recited in amended claim 31. For all of these reasons, Okada does not teach each and every element of the claimed invention. Accordingly, amended claim 31, and claim 32 which depends therefrom, are patentable over Okada.

Also in the Office Action, claims 21-25 and 31-32 have been rejected under 35 USC §103 as unpatentable over Matsuo et al taken with Zamanian and Wolf. With respect to claim 21, the Examiner concedes that "Matsuo fails to show etching in an overetch amount of the substantially vertical component." The Examiner attempts to remedy this deficiency by turning to Zamanian and Wolf. However, as discussed above, Zamanian's conductive layer 32 of polysilicon is not etched at all. It is the barrier layer 34 that is etched. The teachings of Matsuo and Zamanian are not combinable in the manner proposed by the Examiner. Matsuo does not need a multi-layer "pad" that includes a barrier layer. And Zamanian fails to teach overetching of a conductive layer.

Wolf's teachings are directed to the etching of amorphous silicon and silicon dioxide in fluorocarbon-containing plasmas. The Examiner has not demonstrated that any teaching in Wolf has any applicability whatsoever to the method and structure of Matsuo (who uses a high temperature oxide (HTO) and polysilicon). Moreover, Wolf

does not teach the necessity of overetching, simply that a slight amount of overetching may occur in the process taught by Wolf. That is not an explicit teaching that one skilled in the art should overetch in the process of Matsuo. The Examiner has failed to carry his burden of showing evidence of a suggestion or motivation to combine the reference teachings.

With respect to claim 31, as discussed above, no portion of Zamanian's conductive layer 32 has a contact hole etched therein. Nor does Wolf teach or suggest a contact hole in an overlayer that extends into the vertical component of a layer of conductive material. The Examiner concedes that Matsuo also does not. Thus none of the cited references, either taken alone or together teach or suggest the claimed subject matter of claims 31-32. For all of these reasons, applicant submits that claims 21-25 and 31-32 as amended are patentable over Matsuo, Zamanian, and Wolf.

Also in the Office Action, the Examiner rejected claims 21-25 and 31-32 under 35 USC §103 as unpatentable over Okada taken with Zamanian and Toshiyuki. As discussed above, Okada does not teach forming a structure having an opening in a semiconductor layer and filling the opening with a layer of conductive material. The layer of conductive material 9 in Okada's Figs. 2A-C and 3 simply lies upon the semiconductor structure. Contact holes 6 and 6a are filled by electrode material 7a and 7b. An insulating film 8 then overlies the electrodes. Conductive layer 9 is deposited over film 8. No "openings" in film 8 are filled with any conductive material 9. Further, contacts 12 extend only to the surface of conductive layer 9 and do not extend into any vertical component of the conductive layer 9 as recited in amended claim 31.

Thus, even if the reference teachings were to be combined in the manner proposed by the Examiner, the claimed invention would not result. Further, as previously pointed out by applicant, one skilled in the art would not combine the teachings of Toshiyuki with Okada because Toshiyuki teaches away from the methods taught by Zamanian and Okada. For all of these reasons, applicant submits that claims 21-25 and 31-32 as amended are patentable over the cited references.

The claims have been amended for clarity. Applicant submits that the claims are in compliance with §112 and are patentable over the applied art of record. Early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,

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